



Results for "(vangel s.<in>au)"

Your search matched 10 of 1137806 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

[View Session History](#)[New Search](#)

Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

(vangel s.<in>au)

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

Select Article Information

1. 5-GHz 32-bit integer execution core in 130-nm dual-V_{sub} T_I CMOS

Vangal, S.; Anders, M.A.; Borkar, N.; Seligman, E.; Govindarajulu, V.; Erraguntla, V.; Wilson, H.; Pangal, A.; Veeramachaneni, V.; Tschanz, J.W.; Ye, Y.; Somasekhar, D.; Bloechel, B.A.; Dermer, G.E.; Krishnamurthy, R.K.; Soumyanath, K.; Mathew, S.; Narendra, S.G.; Stan, M.R.; Thompson, S.; De, V.; Borkar, S.; Solid-State Circuits, IEEE Journal of Volume 37, Issue 11, Nov. 2002 Page(s):1421 - 1432

[AbstractPlus](#) | [References](#) | Full Text: PDF(1442 KB) IEEE JNL
2. A 28.5 GB/s CMOS non-blocking router for terabit/s connectivity between multiple processors and peripheral I/O nodes

Nair, R.; Borkar, N.Y.; Browning, C.S.; Dermer, G.E.; Erraguntla, V.; Govindarajulu, V.; Pangal, A.; Prijic, J.D.; Rankin, L.; Seligman, E.; Vangal, S.; Wilson, H.A.; Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International 5-7 Feb. 2001 Page(s):224 - 225, 450

[AbstractPlus](#) | Full Text: PDF(320 KB) IEEE CNF
3. Selective node engineering for chip-level soft error rate improvement [in CMOS]

Karnik, T.; Vangal, S.; Veeramachaneni, V.; Hazucha, P.; Erraguntla, V.; Borkar, S.; VLSI Circuits Digest of Technical Papers, 2002. Symposium on 13-15 June 2002 Page(s):204 - 205

[AbstractPlus](#) | Full Text: PDF(260 KB) IEEE CNF
4. A 25 GHz 32 b Integer-execution core in 130 nm dual-V_T CMOS

Vangal, S.; Borkar, N.; Seligman, E.; Govindarajulu, V.; Erraguntla, V.; Wilson, H.; Pangal, A.; Veeramachaneni, V.; Anders, M.; Tschanz, J.; Ye, Y.; Somasekhar, D.; Bloechel, B.; Dermer, G.; Krishnamurthy, R.; Narendra, S.; Stan, M.; Thompson, S.; De, V.; Borkar, S.; Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International Volume 1, 3-7 Feb. 2002 Page(s):412 - 478 vol.1

[AbstractPlus](#) | Full Text: PDF(427 KB) IEEE CNF
5. 1.1 V 1 GHz communications router with on-chip body bias in 150 nm CMOS

Narendra, S.; Haycock, M.; Govindarajulu, V.; Erraguntla, V.; Wilson, H.; Vangal, S.; Pangal, A.; Seligman, E.; Nair, R.; Keshavarzi, A.; Bloechel, B.; Dermer, G.; Mooney, R.; Borkar, N.; Borkar, S.; De, V.; Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International Volume 1, 3-7 Feb. 2002 Page(s):270 - 466 vol.1

[AbstractPlus](#) | Full Text: PDF(472 KB) IEEE CNF
6. 5GHz 32b Integer-execution core in 130nm dual-V_{sub} T_I CMOS

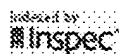
Vangal, S.; Borkar, N.; Seligman, E.; Govindarajulu, V.; Erraguntla, V.; Wilson, H.; Pangal, A.; Veeramachaneni, V.; Anders, M.; Tschanz, J.; Ye, Y.; Somasekhar, D.; Bloechel, B.; Dermer, G.; Krishnamurthy, R.; Narendra, S.; Stan, M.; Thompson, S.; De, V.; Borkar, S.; Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International Volume 2, Feb 3-7, 2002 Page(s):334 - 535

[AbstractPlus](#) | Full Text: PDF(488 KB) IEEE CNF
7. 1.1V 1GHz communications router with on-chip body bias in 150nm CMOS

Narendra, S.; Haycock, M.; Govindarajulu, V.; Erraguntla, V.; Wilson, H.; Vangal, S.; Pangal, A.; Seligman, E.; Nair, R.; Keshavarzi, A.; Bloechel, B.; Dermer, G.; Mooney, R.; Borkar, N.; Borkar, S.; Vivek De; Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International Volume 2, Feb 3-7, 2002 Page(s):218 - 482

[AbstractPlus](#) | Full Text: PDF(521 KB) IEEE CNF

8. **A 5 GHz floating point multiply-accumulator in 90 nm dual V/sub T/ CMOS**
Vangal, S.; Hoskote, Y.; Somasekhar, D.; Erraguntla, V.; Howard, J.; Ruhl, G.; Veeramachaneni, V.; Finan, D.; Mathew, S.; Borkar, N.;
Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International
2003 Page(s):334 - 497 vol.1
[AbstractPlus](#) | Full Text: [PDF](#)(374 KB) | [Multimedia](#) IEEE CNF
9. **A 10GHz TCP offload accelerator for 10Gb/s Ethernet in 90nm dual-V/sub T/ CMOS**
Hoskote, Y.; Erraguntla, V.; Finan, D.; Howard, J.; Klowden, D.; Narendra, S.; Ruhl, G.; Tschanz, J.; Vangal, S.; Veeramachaneni, V.; Wilson, H.; Jianping Xu; Borkar, N.;
Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International
2003 Page(s):258 - 492 vol.1
[AbstractPlus](#) | Full Text: [PDF](#)(741 KB) | [Multimedia](#) IEEE CNF
10. **Ultra-low voltage circuits and processor in 180nm to 90nm technologies with a swapped-body biasing technique**
Narendra, S.; Tschanz, J.; Hofsheier, J.; Bloechel, B.; Vangal, S.; Hoskote, Y.; Tang, S.; Somasekhar, D.; Keshavarzi, A.; Erraguntla, V.; Dermer, G.; Borkar, N.; Borkar, S.; De, V.;
Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International
15-19 Feb. 2004 Page(s):156 - 518 Vol.1
[AbstractPlus](#) | Full Text: [PDF](#)(606 KB) | [Multimedia](#) IEEE CNF

[View Selected Items](#)[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2005 IEEE - All Rights Reserved

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	28	("6360189" "6018756" "6397239" "6397240" "20040225703" "6578060" "6578063" "5978827" "5993051" "6175851" "6480872" "6529928" "6571267" "6584485").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 10:57
L2	6	("5764089" "5898330" "5900759").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 10:57
L3	34	1 or 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:41
L4	2	"6205462".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 11:15
L5	2	"6542915".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 11:15
L6	23303	"708"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:41
L7	2539	((floating adj point\$1) or floating-point\$1) and (multiplier\$1 or multiplication or multiplying) and conver\$5 and normaliz\$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:42
L8	554	7 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:42
L9	509	8 and @ad<"20010604"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:42

L10	75	weight\$1 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:43
L11	22	(conver\$7.ti. or conver\$7.clm. or conver\$7.ab.) and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/29 13:43